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Alexandria, ~~VA 22313~~-1450

Attorney for Appellants

Date: 14 November 2008

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	10/002,461
Applicant	:	SLAVIN, Keith R.
Filed	:	01 November 2001
Titled	:	Low Power, Hash-Content Addressable Memory Architecture
Art Unit	:	2189
Examiner	:	ELMORE, Reba I.
Atty. Docket No.	:	PAT000955-000 (013721-0110-999)

TRANSMITTAL LETTER

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In support of Appellant's Notice of Appeal from the Examiner to the Board of Patent Appeals and Interferences filed in the above-captioned application, enclosed is the following:

- Appellant's Brief on Appeal Under 37 C.F.R. § 41.37

Please charge Deposit Account No. 50-3013 in the amount of $540 to cover the requisite fees. The Commissioner is hereby authorized to charge any underpayment or credit any overpayment to our Deposit Account No. 50-3013.

Respectfully submitted,

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Date: 14 November 2008

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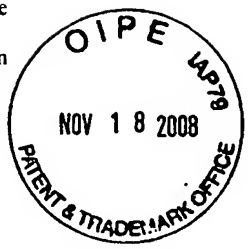

Attorney for Appellants

Date: 14 November 2008

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APPELLANT'S BRIEF ON APPEAL UNDER 37 C.F.R. § 41.37

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This appeal brief is in support of Appellant's Notice of Appeal from the Examiner to the Board of Patent Appeals and Interferences mailed on 3 September 2008 and is filed pursuant to 37 C.F.R. § 41.37.

(i) REAL PARTY IN INTEREST

The real party in interest in this case is Micron Technology, Inc., the assignee of the entire interest of the above-identified patent application.

(ii) RELATED APPEALS AND INTERFERENCES

There are no known prior or pending appeals, interferences, or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(iii) STATUS OF CLAIMS

Claims 1-38 and 41-44, which are all of the claims in the application, stand finally rejected in the final Office action mailed on June 13, 2008. The rejection of claims 1-38 and 41-44 is appealed herein. The claims, as they presently stand, are found in the Claims Appendix to this Appellant's Appeal Brief.

(iv) STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final Office action.

(v) SUMMARY OF CLAIMED SUBJECT MATTER

The invention is directed to solving a problem inherent in the operation of content-addressable memories (CAMs). A CAM is a memory that operates the opposite of a random access memory (RAM). In a RAM, you input an address and the data stored at that address is output. In a CAM, you input the data, and an address corresponding to that date is output. For highest performance, conventional CAM architectures simultaneously compare all of their data entries with the data on an input bus. To enable simultaneous comparison, each memory cell must have its own comparison logic to detect a match. That greatly increases power consumption as every comparison circuit is active on every clock cycle. [0004][1]

FIG. 6 of the instant application shows a typical CAM row 10 as having n CAM cells 12(1)-12(n) each coupled to an associated match line ML. A pull-up transistor 14, coupled between a supply voltage VDD and match line ML, has a gate tied to ground potential, and therefore remains in a conductive state. Prior to each compare operation between an n-bit comparand word and an n-bit CAM word stored in CAM cells 12(1)-12(n), match line ML is precharged to supply voltage VDD via pull-up transistor 14. The n-bits of the comparand word are compared with corresponding bits of the CAM word in respective CAM cells 12(1)-12(n). If all bits of the comparand word match corresponding bits of the CAM word, the match line ML

[1] Paragraph references are to the published application.

remains charged to indicate a match condition. Conversely, if one of the comparand bits does not match the corresponding CAM bit, the CAM cell 12 storing that CAM bit discharges match line ML toward ground potential to indicate a mismatch condition. [0009]

The match lines in a CAM array are typically precharged to the supply voltage VDD for *each and every compare operation.* Thus, for each mismatch condition, an associated match line ML is first charged toward VDD and then discharged toward ground potential. Current flow associated with this charging and discharging results in undesirable power consumption. Further, as the number of CAM cells in each row of a CAM array increases, capacitive loading on the match lines increases accordingly. As loading on the match lines increases, the current required to charge the match lines toward the supply voltage increases. Accordingly, as CAM words are widened, for example, to accommodate longer internet addresses, power consumption resulting from charging the match lines during compare operations may significantly increase. Furthermore, because mismatches are far more common than matches, as internet addresses are lengthened and CAM words widened, power consumption increases substantially. [0010]

The present invention includes an apparatus and a method of reducing the match line pre-charging activity for a CAM access while allowing operation at the highest possible CAM speeds. The method involves sending a comparand word to a CAM and also sending the comparand word to a set of hash circuits, one for each legal prefix length, for parallel comparisons. Each hash circuit output then goes to the address of a corresponding memory look-up *which defines a region of the CAM* in which, according to the known hashing behavior, a match is guaranteed to be located--if such a match exists as a CAM entry. *Thus, by selectively energizing only those regions of the CAM where a match is guaranteed to exist, instead of the entire CAM, energy consumption is reduced.* If more (including up to all) of the CAM is enabled than is necessary, then the CAM will still work normally, but useless entry matching will occur and CAM power savings will fall. [0011]

The method of the present invention is described in claim 1 which recites inputting an input word to a plurality of hash circuits, each hash circuit being responsive to a different portion of the input word. See [0021] and the input lines to elements 24(1)-24(n) in FIG. 1. A hash signal is output from each hash circuit. See [0021] and the output lines from elements 24(1) to 24(n) in FIG. 1. A *portion* of the CAM is enabled in response to the hash signals. See [0021] and the enable lines output from element 26 in FIG. 1. The input word is input to the CAM. See

the [0021] and input line to element 20 from element 28. The input word is compared in the *enabled portions* of the CAM. This is how element 20 operates. See [0021]. Information is output in response to the comparing. See the output from element 20.

Independent claim 8 is a subset of claim 1 in that claim 8 recites a method of operating a CAM, comprising hashing a comparand word (see 24(1) – 24(n) in FIG. 1), precharging certain portions of a CAM in response to said hashing (see the enable lines output from element 26) which, in turn, is responsive the hash/SRAM circuits, and inputting the comparand word to the CAM. See the input line to element 20 from element 28. See also [0021].

Independent claim 15 is similar to claim 1, but is specific about the input being an internet address and refers to comparing the address in only the identified portion of the CAM instead of the energized portion of the CAM. See [0022].

Independent claim 22 is similar to claim 1 and recites a method of operating a CAM for processing address information, comprising: hashing different prefixes within an internet address; precharging certain portions of a CAM in response to the hashing; comparing the internet address in the precharged portions of the CAM; and outputting information in response to a match being found in the CAM. See [0021] and [0022].

Independent claim 28 is an apparatus claim that recites a circuit, comprising a CAM (20) for receiving a comparand word; a plurality of hash circuits (24(1)-24(n)) connected in parallel, each for producing a hash signal in response to a portion of the comparand word; and a circuit (26) responsive to said hash signals, for precharging portions of the CAM. See [0021].

Independent claim 34 is similar to claim 28 but is more detailed. Independent claim 34 recites a circuit, comprising: a CAM (20) (See [0021]); a plurality of hash circuits (40(1)-40(n) in FIG. 2) each for producing a hash signal in response to a portion of a comparand word (See [0026]); a plurality of memory devices (42(1)-42(n)) responsive to said hash circuits (See [0028]); enable logic (26), responsive to said plurality of memory devices, for enabling portions of said CAM (See [0021]); and a delay circuit (28) for inputting the comparand word to said CAM (See [0021]).

The last independent claim, claim 41, is somewhat different than the other independent claims because claim 41 is directed to a method of initializing hardware having a CAM divided into a plurality of banks comprising: transferring network addresses to the CAM based on an index to a hash table (See 86, FIG. 4, and [0057]); transferring port numbers to an output

memory device responsive to the CAM (See 88, FIG. 4, and [0057]); modifying bit prefix values to obtain a ternary representation (See 92, FIG. 4, and [0057]); calculating bank run length information (See 94, FIG. 4, and [0057]); and loading bank starting address and bank run length information into a plurality of memory devices (See 96, FIG. 4, and [0057]).

(vi) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. 35 U.S.C. § 112, First Paragraph

In paragraph 7 of the Office action, claims 1-38 and 41-44 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. It is the examiner's position that the delay circuit is not adequately disclosed.

B. 35 U.S.C. § 102

In paragraph 10 of the Office action, claims 41-44 stand rejected as being anticipated by Cheriton (U.S. Patent No. 7,002,965 "Cheriton").

C. 35 U.S.C. § 103

In paragraph 15 of the Office action, claims 1-38 stand rejected as being obvious over Hariguchi et al. (U.S. Patent No. 6,665,297 "Hariguchi") in view of Cheriton.

Each of these grounds of rejection is respectfully traversed. As to the art rejections, the Office has failed to demonstrate that any of the applied references teaches or suggests reducing the power consumed by a CAM by enabling only those portions of a CAM where a match is guaranteed to occur.

(vii) ARGUMENT

A. The rejection under 35 U.S.C. § 112, first paragraph, is improper and should be reversed.

1. The Office has failed to provide any basis for a rejection of claims 1-3, 6-10, 12-17, 19-23, 25-33, and 41-44, under 35 U.S.C. § 112, first paragraph.

There is no explanation in the Office action as to why claims 1-3, 6-10, 12-17,[2] 19-23, 25-33, and 41-44 are rejected under U.S.C. § 112, first paragraph. The allegedly unsupported recitation (the delay element) does not appear in claims 1-3, 6-10, 12-17, 19-23, 25-33, and 41-44. As to those claims, the rejection should be reversed.

2. The examiner has misunderstood the invention and applied an incorrect standard in the 35 U.S.C. § 112, first paragraph, rejection.

In support of rejection under 35 U.S.C. § 112, first paragraph, the examiner states the following:

> If memory elements are not limited as to which types can be used and steps or instructions are not limited as to what step or instruction is performed, if the only 'teaching' is one or [*sic* of] ordinary skill in the art already knows how to make and use, then where is the inventiveness of the present invention? Office action, p. 3, ¶ 9.

The examiner has clearly not perceived that the present invention is directed to a method and apparatus for enabling a CAM to be operated in a power saving manner. That invention is adequately disclosed. If the invention was directed to some new type of delay circuit, or some method of synchronization of signals being input to a CAM, then perhaps the examiner's rejection would have some merit. However, it is the claims which define the invention, and it is the claims for which the specification must be enabling.

Additionally, recitation of a delay step is analogous to the recitation of the step of amplifying a signal. Where the invention is not directed to a new type of amplifier, no one can seriously suggest that for an amplifying step to be enabled, there must be a disclosure of how the

[2] The Office action incorrectly identifies claim 17 as containing a "delaying" step. Claim 18 contains the "delaying" step.

transistors forming the amplifier are biased, or what the gain of the amplifier must be. Surely those types of implementation details are well known to persons of ordinary skill in the art. Where components and steps such as delaying and amplifying are not the focus of the invention, nothing more than a generic recitation is needed. Indeed, the examiner, in a prior art rejection (see Office action, first full paragraph on page 8), cites nothing more than a "router control procedure" as a teaching for delaying the inputting of the comparand word. In fact, nowhere in the router control procedure is "delaying" mentioned.

Further, it is respectfully submitted that the time required to enable or precharge a CAM would be readily apparent to a person of ordinary skill in the art based on the specifications for the memory such that experimentation would be unnecessary. Knowing the time needed to precharge the memory based on the memory's specifications, those of ordinary skill in the memory art would be easily capable of designing a circuit to provide the necessary delay. For example, when command signals are received in a memory in advance of address signals, it is well known in the art that the execution of the command signals must be coordinated with the decoding of the address signals. For the examiner to state that a person of ordinary skill in the memory art would not know how to construct a delay circuit based on known precharging times is completely without foundation in the record. Applicant respectfully notes that specifications are written for persons of ordinary skill in the art and preferably omit details that are well known to such persons. *Genetech, Inc. v. Novo Nordisk A/S*, 108 F.3d 1361 (Fed. Cir. 1997).

The examiner's citation of *Automotive Technologies International, Inc. v. BMS of North America, Inc.*, 501 F.3d 1274 (Fed. Cir. 2007) does not support the examiner's position for at least the following reasons:

- That case involved a situation where a mechanical side impact sensor was disclosed in detail but the claims recited an electronic side impact sensor. There is no dichotomy in the instant application between what is disclosed and what is claimed. And what is claimed is claimed in no more detail than what is disclosed.
- The court in that case stated that "the novel aspect of this invention is using a velocity-type sensor for side impact sensing." Thus, the specification in the case cited by the examiner was silent precisely at the "point of novelty." The instant applicant has neither in the specification nor during prosecution argued that the delay

circuit is novel or that the delay circuit is the "point of novelty" or even "essential subject matter."

- The specification in the case cited by the examiner stated that side impact sensing is a new field. There is no corresponding statement in this case that the construction of delay circuits is a new field.
- The court had testimony that indicated that a "great deal of experimentation" would have been necessary to make an electronic side impact sensor after reading the specification in the case cited by the examiner. No evidence that a great deal of experimentation would be required to construct a delay circuit is in the record in the instant application.

For the foregoing reasons it is respectfully requested that the rejection of claims 1-38 and 41-44 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement, be reversed.

B1. The rejection of claims 41-44 as being anticipated by Cheriton is not correct.

For anticipation, the reference must disclose each and every limitation of the claim. If even one limitation is not disclosed, the rejection must be reversed.

Claims 41-44 recite "calculating bank run length information." The bank run length information, along with a start index, identifies the portion of the CAM that is to be enabled. See paragraph [0057]. The examiner cites Cheriton, col. 6, lines 43-49, as teaching that limitation. That portion of Cheriton provides:

> FIG. 3 illustrates a block diagram of one exemplary embodiment including one or more TCAMs 301 for handling input and output classification (e.g., for ACLs, QoS, NAT, encryption, etc.) for a packet or packet header stored in packet buffer 300. This illustrated embodiment also includes one or more forwarding CAMs 305 to classify packets for IP forwarding decisions.

The cited portion of Cheriton fails to disclose calculating bank run length information. The failure of Cheriton to disclose this limitation is expected because Cheriton does not disclose

or suggest enabling a portion of a CAM and therefore does not initialize its CAM in the same manner as is claimed. The anticipation rejection must be reversed.

Claims 41-44 recite "loading starting address and bank run length information into a plurality of memory devices." The examiner cites Cheriton, col. 6, line 43 to col. 7, line 21, as teaching that limitation. That portion of Cheriton provides:

> FIG. 3 illustrates a block diagram of one exemplary embodiment including one or more TCAMs 301 for handling input and output classification (e.g., for ACLs, QoS, NAT, encryption, etc.) for a packet or packet header stored in packet buffer 300. This illustrated embodiment also includes one or more forwarding CAMs 305 to classify packets for IP forwarding decisions.
>
> On packet reception, the packet flow label is extracted from the received packet and passed to the classification TCAMs 301. In one embodiment, TCAMs 301 typically accept a full flow label including IP source and destination addresses, protocol type, flags and layer 4 source and destination ports, a virtual local area network (VLAN) id and/or other fields. The system includes a hash directory of flow labels implemented in a large SRAM memory 302, suitable for flow classification for netflow statistics, microflow policing and redirection. Using on-chip SRAM, this hash directory may be implemented, for example, as a 16-set associative hash table, effectively implementing a binary associative memory. In one embodiment, TCAMs 301 produce an index which is used by classification memory 302 to return an entry that provides indications on forwarding, policing and/or other packet classification indications.
>
> In one embodiment, the full flow label of the packet is then masked off by mask generator 303. A mask is typically selected based on other classifications applied to the packet, including classification produced by TCAM 301. The masked flow label is then used as the hashing key, and a lookup operation is performed in the hash directory using this mask in hash function 304. In one embodiment, a CAM or other lookup structure (e.g., TRIE) is used in place or, or in addition to the hash table. If a matching hash directory entry is found by hash function 304, the handling specified by this directory entry is used by one or more CAMs 305 to generate one or more classification indications and overriding the relevant handling that may have been determined by earlier packet classification mechanisms. If the one or more CAMs 305 may generate multiple classification indications, selection logic 306 is used to select between the classification indications, and to

> generate the packet classification 307. Additionally, selection logic 306 may further receive and use the result of generated *[sic]* by TCAMs 301 in making its selection. For example, in one embodiment, TCAMs 301 may generate a forwarding and/or policing decision, and CAMs 305 may be used to override this generated forwarding and/or policing decision.

On its face, the cited portion of Cheriton deals with packets on reception, not the initialization of the hardware. The cited portion of Cheriton discusses masking full flow labels upon reception, and not loading starting address and bank run length information into a plurality of memory devices. The failure of Cheriton to disclose this limitation is expected because Cheriton does not disclose or suggest enabling a portion of a CAM and therefore does not initialize its CAM in the same manner as is claimed. The anticipation rejection must be reversed.

B2. The rejection of claim 44 as being anticipated by Cheriton is not correct.

Claim 44 recites "wherein said bank run length information includes one of a bank end address and a bank address span." The examiner cites the same portion of Cheriton (i.e., col. 6, line 43 to col. 7, line 21) as teaching that limitation. As seen from the above quote, that teaching is not found. The failure of Cheriton to disclose this limitation is expected because Cheriton does not disclose or suggest enabling a portion of a CAM and therefore does not initialize its CAM in the same manner as is claimed. The anticipation rejection must be reversed.

C1. The rejection of claims 1, 8, 15, 22, 28, and 34 as being obvious over Hariguchi et al. (U.S. Patent No. 6,665,297 "Hariguchi") in view of Cheriton is inconsistent and incorrect and should be reversed.

On page 6 of the Office action, the examiner states that Hariguchi teaches:

> enabling or precharging portions of a CAM in response to the hash signals as portions of the CAM being enabled when the hash signals indicating the CAM has a match of the prefix (e.g., see column 7, line 50 to column 8, line 3).

On page 7 of the Office action, the examiner contradicts herself by stating:

> Hariguchi teaches the limitations of the independent claims as given above, however, the primary reference does not specifically teach using hash signals to enable portions of a CAM.

This inconsistency, on its face, indicates a failure of the Office to properly perceive and clearly state what the primary reference teaches. For that reason, the obviousness rejection should be withdrawn.

Turning to the merits of the examiner's contention as set forth on page 6 of the Office action, the relevant portion of Hariguchi, column 7, line 50 to column 8, line 3, provides as follows:

> During a third pipeline clock cycle, in the selection stage 88, a priority encoder 170 identifies the output pointer associated with the longest match among the hash circuits 82 (FIG. 2) and CAM 80. The priority encoder 170 receives the hash circuit hit/miss flags (H/M/32 . . . H/M/8) from the hash circuits 82 (FIG. 2) and the CAM hit/miss (H/M) flag from the CAM 80. The priority encoder 170 also receives the prefix length of the match from the CAM 80. The hit/miss flags from each hash bucket circuit are input to predetermined lines of the priority encoder 170 such that each line corresponds to the unmasked prefix length of that hash bucket circuit. In the priority encoder 170, a hash match register 171 includes a hash hit/miss flag, a matching hash address, and the matched hash prefix length. When the CAM 80 has the prefix length indicating the longest match, the priority encoder 170 outputs a CAM/hash select signal indicating the CAM. When one of the hash circuits has the longest match, the priority encoder 170 outputs a CAM/hash select signal indicating the hash circuits and also outputs a longest match select code signal corresponding to the hash circuit having the longest match.

It is clear from this quotation that this section of Hariguchi deals with identifying the component where the longest match is found and not enabling or precharging portions of a CAM in response to the hash signals. As can be seen clearly from Fig. 2A of Hariguchi, the hash circuits are in parallel with the content addressable memory 80. The selection stage 88 receives inputs from all of the hash circuits as well as the content addressable memory 80. See Hariguchi, col. 5, lines 15-32. Thus, Hariguchi fails to disclose precharging portions of a CAM in response to the hash signals.

The examiner then turns to the secondary reference, Cheriton, as teaching "using a hash function to enable or choose portions of a CAM as generating classification indications which allows for packet classification in network routers," citing Figure 3, and col. 6, line 43 to col. 7,

line 21, reproduced above. Cheriton, in no way teaches using a hash function to enable or choose portions of a CAM.

Cheriton discloses a TCAM/CAM classifier for classifying and routing data packets. The TCAM/CAM classifier has a CAM (See figure 3, Ref. No. 305) that stores a hash directory of network IP addresses. The CAM performs a comparison between a received hash index based on a flow label of a data packet and the entire hash directory of network IP addresses. The CAM selects the network IP address for routing the data packet based on a match during the comparison of the received hash index and the entire hash directory of network IP addresses (See col. 3, lines 18-21, and col. 6, lines 47-49). The cited portions of Cheriton do not teach using hashing signals to enable portions of a CAM and instead teach the entire CAM being responsive to hash signals. Therefore, modifying the router disclosed by Hariguchi to contain a CAM responsive to hash signals instead of destination addresses does not teach or suggest enabling portions of the CAM in response to the hash signals, but rather the modification teaches an entire CAM being responsive to a different type of input signal. Combining the teachings of the two references does not produce the benefit of reduced power saving achieved by the claimed invention. Accordingly, it is believed that claims 1-38 are in condition for allowance.

C2. The rejection of claims 4, 11, 18, and 24 as being obvious over Hariguchi et al. in view of Cheriton is incorrect and should be reversed.

On page 8 of the Office action, the examiner indicates that "Hariguchi teaches delaying the inputting of the input word or comparand word to the CAM until the enabling or precharging is completed as part of the router control procedure which is stored in the memory for controlling the overall operation of the router," citing col. 4, lines 31-62. That portion of Hariguchi does disclose a router control procedure that states that it "controls the overall operation of the router 26." There is, however, no mention of a delay. The failure to mention a delay is not surprising because in the prior art, as discussed in the instant application at [0009], the match lines are always precharged. Therefore, the primary reference is defective such that the combination of references fails to render obvious claims 4, 11, 18, and 24.

It is also interesting to note, as mentioned above in conjunction with the § 112 rejection, that the examiner finds a reference to a router control procedure that controls the overall operation of the router to be a sufficient disclosure for delaying the inputting of the input word

yet, in contrast, finds applicant's specification that explicitly mentions the delay and illustrates the delay in the drawing as not complying with the written description requirement. If a delay can be taught by the mere mention of a router control procedure, then surely a delay can be taught by explicitly showing the delay in the figure and describing the purpose of the delay in the specification.

C3. The rejection of claims 5, 17, 19, and 25 as being obvious over Hariguchi in view of Cheriton is incorrect and should be reversed.

Each of the dependent claims 5, 17, 19, and 25 recites precharging *portions* of the CAM. The examiner cites col. 4, line 63 to col. 5, line 14, of Hariguchi as teaching this limitation. The cited portion of Hariguchi is the description of the router 26 and router control procedure. There is no disclosure in that portion, or any other portion, of Hariguchi that teaches enabling portions of a CAM. In addition, this ground of rejection is inconsistent with page 7 of the Office action in which the examiner indicates that Hariguchi, the primary reference, "does not specifically teach using hash signals to enable portions of a CAM." As discussed above in connection with the independent claims, both Hariguchi and Cheriton are silent with respect to this limitation. Accordingly, the rejection of claims 5, 17, 19, and 25 should be reversed.

C4. The rejection of claims 6-7, 13-14, 20-21, and 26-27 as being obvious over Hariguchi in view of Cheriton is incorrect and should be reversed.

The examiner provides the following logic to support this ground of rejection:

> Hariguchi does not specifically teach the stored signals include using a run length or ending index in conjunction with a starting index, however, the reference does teach using a starting index to help select a network destination for the sending of a datagram. Sending a datagram means the length of the data to be sent must also be specified or known which indicates using either a run length or an ending index for the determination of a message length because the purpose of the invention as taught by Hariguchi is to select an Internet address for sending a datagram or message which means sending not only the address information but also sending the length of the datagram whether the length is conveyed as a run length or as an ending index.

This logic has absolutely nothing to do with the starting index, run length, and ending index recited in these dependent claims. These limitations are related to the portions of the CAM which are precharged. As previously discussed, Hariguchi does not precharge only portions of the CAMs used in his device. Therefore, a starting index, ending index, or run length for identifying those portions of the CAM which are to be precharged has no meaning within the context of Hariguchi. The rejection of claims 6-7, 13-14, 20-21, and 26-27 should be reversed.

CONCLUSION

For the foregoing reasons, it is respectfully requested that the rejection of all of the claims be reversed.

Respectfully submitted,

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(viii) CLAIMS APPENDIX

1. A method, comprising:

inputting an input word to a plurality of hash circuits, each hash circuit being responsive to a different portion of said input word;

outputting a hash signal from each hash circuit;

enabling portions of a CAM in response to said hash signals;

inputting said input word to said CAM;

comparing said input word in the enabled portions of said CAM; and

outputting information responsive to said comparing.

2. The method of claim 1 additionally comprising assigning a mask to each hash circuit such that each hash circuit is responsive to a different n-bit portion of said input word.

3. The method of claim 1 additionally comprising inputting the least significant n bits of said input word to a memory, and wherein said outputting includes selecting between information responsive to a match being found in said memory and information responsive to a match being found in said CAM.

4. The method of claim 1 additionally comprising delaying the inputting of said input word to said CAM until said enabling is completed.

5. The method of claim 1 wherein said enabling includes using said hash signals to select from a plurality of stored signals, and using the selected stored signals to enable a portion of said CAM.

6. The method of claim 5 wherein said using the selected stored signals includes using a starting index and a run length.

7. The method of claim 5 wherein said using the selected stored signals includes using a

starting index and an ending index.

8. A method of operating a CAM, comprising:

hashing a comparand word;

precharging certain portions of a CAM in response to said hashing; and

inputting said comparand word to said CAM.

9. The method of claim 8 wherein said hashing includes hashing different n-bit portions of said comparand word.

10. The method of claim 8 additionally comprising inputting the least significant n bits of said comparand word to a memory, and outputting information responsive to one of a match being found in said memory and a match being found in said CAM.

11. The method of claim 8 additionally comprising delaying the inputting of said comparand word to said CAM until said precharging is completed.

12. The method of claim 8 wherein said precharging includes using said hash signals to select from a plurality of stored signals, and using the selected stored signals to precharge portions of said CAM.

13. The method of claim 12 wherein said using the selected stored signals includes using a starting index and a run length.

14. The method of claim 12 wherein said using the selected stored signals includes using a starting index and an ending index.

15. A method of operating a CAM for processing address information, comprising:

inputting an Internet address to a plurality of hash circuits, each hash circuit being responsive to a different portion of said address;

outputting a hash signal from each hash circuit;

using said hash signals to identify portions of a CAM;
inputting said address to said CAM;
comparing said address in only the identified portions of said CAM; and
outputting port information in response to a match being found in said CAM.

16. The method of claim 15 additionally comprising assigning a mask to each hash circuit such that each hash circuit is responsive to a different n-bit portion of said address.

17. The method of claim 15 additionally comprising inputting the least significant n bits of said address to a memory, and wherein said outputting includes selecting between port information associated with a match in said memory and port information associated with a match in said CAM.

18. The method of claim 15 additionally comprising delaying the inputting of said address to said CAM until portions of said CAM have been precharged in response to said hash signals.

19. The method of claim 15 wherein said using said hash signals includes using said hash signals to select from a plurality of stored signals, and using the selected stored signals to precharge portions of said CAM.

20. The method of claim 19 wherein said using the selected stored signals includes using a starting index and a run length.

21. The method of claim 19 wherein said using the selected stored signals includes using a starting index and an ending index.

22. A method of operating a CAM for processing address information, comprising:
hashing different prefixes within an Internet address;
precharging certain portions of a CAM in response to said hashing;
comparing said Internet address in said precharged portions of the CAM; and

outputting information in response to a match being found in the CAM.

23. The method of claim 22 additionally comprising inputting the least significant n bits of said address to a memory, and wherein said outputting information includes selecting between information associated with a match in said memory and information associated with a match in said CAM.

24. The method of claim 22 additionally comprising delaying said comparing until said precharging is completed.

25. The method of claim 22 wherein said precharging includes using said hash signals to select from a plurality of stored signals, and using the selected stored signals to precharge portions of the CAM.

26. The method of claim 25 wherein said using the selected stored signals includes using a starting index and a run length.

27. The method of claim 25 wherein said using the selected stored signals includes using a starting index and an ending index.

28. A circuit, comprising:

a CAM for receiving a comparand word;

a plurality of hash circuits connected in parallel, each for producing a hash signal in response to a portion of the comparand word; and

a circuit, responsive to said hash signals, for precharging portions of said CAM.

29. The circuit of claim 28 wherein said circuit responsive to said hash signals includes a plurality of memory devices responsive to said hash signals and enable logic responsive to said plurality of memories.

30. The circuit of claim 29 wherein said plurality of memory devices includes a plurality of

SRAMs.

31. The circuit of claim 28 additionally comprising an output memory device responsive to said CAM for outputting information in response to a match in said CAM.

32. The circuit of claim 31 additionally comprising an input memory device responsive to a portion of the comparand word, and a switch responsive to said input memory device and said output memory device.

33. The circuit of claim 28 additionally comprising a processor, said CAM, said plurality of hash circuits, and said circuit responsive to said hash circuits receiving information from said processor.

34. A circuit, comprising:

a CAM;

a plurality of hash circuits each for producing a hash signal in response to a portion of a comparand word;

a plurality of memory devices responsive to said hash circuits;

enable logic, responsive to said plurality of memory devices, for enabling portions of said CAM; and

a delay circuit for inputting the comparand word to said CAM.

35. The circuit of claim 34 wherein said plurality of memory devices includes a plurality of SRAMs.

36. The circuit of claim 34 additionally comprising an output memory device responsive to said CAM for outputting information in response to a match in said CAM.

37. The circuit of claim 36 additionally comprising an input memory device responsive to a portion of the comparand word, and a switch responsive to said input memory device and said output memory device.

38. The circuit of claim 34 additionally comprising a processor for initializing said hash circuits, said plurality of memory devices and said CAM.

39. - 40. (Cancelled)

41. A method of initializing hardware having a CAM divided into a plurality of banks, said method comprising:

transferring network addresses to the CAM based on an index to a hash table;

transferring port numbers to an output memory device responsive to the CAM;

modifying bit prefix values to obtain a ternary representation;

calculating bank run length information; and

loading bank starting address and bank run length information into a plurality of memory devices.

42. The method of claim 41 additionally comprising periodically transferring invalid network addresses to the CAM.

43. The method of claim 41 additionally comprising transferring port information to an SRAM for prefixes below a certain length.

44. The method of claim 41 wherein said bank run length information includes one of a bank end address and a bank address span.

(ix) EVIDENCE APPENDIX

None.

(x) RELATED PROCEEDINGS APPENDIX

None.